Notice of Allowability	Application No.	Applicant(s)	
	09/873,038	LAL, SANJAY	
	Examiner	Art Unit	
	Haresh Patel	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/27/2005*.

2. ☒ The allowed claim(s) is/are *1,3-12,14-16,21 and 23-27*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *3/9/2006* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

EXAMINER'S AMENDMENT

1. Claims 1, 3-12, 14-16, 21 and 23-27 are presented for examination. Claims 2, 13, 17-20, 22 and 28-39 are cancelled.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Authorization for this examiner's amendment was given in a telephone interview with Mr. Kevin G. Shao on 03/20/2006.

Amendments to the Specification

4. Please amend the specification as following:

a) page 13, line 2, after "machine" add --as storage medium or transmission medium--

b) page 13, line 3, replace "machine-readable" with --storage--

c) page 13, line 5, replace "memory devices," with --memory devices. The transmission medium includes--

Amendments to the Claims

5. Please cancel claims 2, 13 and 22.

6. Please amend claims 1, 3, 12, 21, 23-27 as shown below.

Claim 1 (Currently Amended): A method for handling exceptions in a multi-processor system, the method comprising:

receiving an exception within a processor which is one of a plurality of processors of the multi-processor system which is implemented within a control card of a network element for routine data in networks, wherein each of the plurality of processors in the multi-processor system shares a memory within the multi-processor system, wherein the memory includes a common interrupt handling vector address space shared by the plurality of the processors and a dedicated interrupt handling vector address space for each of the plurality of the processors, and

executing one or more instructions at an address associated with a type of the received exception within the common interrupt handling vector address space of the memory, wherein the one or more instructions cause the processor to modify based on an identification of the processor an execution flow of the received exception to execute an interrupt handler located within a respective dedicated interrupt handling vector address spaces associated with the processor,

wherein the plurality of processors includes a first processor and a second processor, the first processor executing a first operating system and the second processor executing a second operating system, the second operating system being different from the first operating systems and wherein the first processor along with the first operating system is configured to handle routine of data received within the network element and the second processor along with the second operating system is configured to handle provisioning and configuration of the network element;

wherein the first operating system is a real-time operating system handling the routing of data within the network element and the second operating system is a non real-time operating system handling the provisioning and configuration of the network element.

Claim 3 (Currently Amended): The method of claim 12, wherein the first operating systems is associated with a first dedicated interrupt handling vector address spaces associated with a the first processor, and wherein the second operating system is associated with a second dedicated interrupt handling vector address space associated with the second processor.

Claim 12 (Currently Amended): A system comprising:

a plurality of processors including a first processor and a second processor implemented within a control card of a network element for routing data for networks;

a memory that includes

a common exception handling vector address space shared by the plurality of processors, and

a plurality of exception handling vector address spaces each associated with each of the plurality of processors, including a first exception handling vector address space and a second exception handling vector address space associated with the first processor and second processor respectively;

a memory controller coupled to the memory and the plurality of processors, wherein the first processor is to execute a first operating system,

wherein the second processor is to execute a second operating system, the second processor to execute one or more instructions in the common exception handling vector address space upon receipt of an exception, wherein the one or more instructions cause the second processor to modify based on an identification of the second processor an execution flow of the exception to execute an interrupt handler located within a respective dedicated interrupt handling vector address spaces associated with the second processor,

wherein ~~the~~ the second operating system is different from the first operating system, and wherein the first processor along with the first operating system is configured to handle routing of data received within the network element and the second processor along with the second operating system is configured to handle provisioning and configuration of the network element;

wherein the first operating system is a real-time operating system handling the routing of data within the network element and the second operating system is a non real-time operating system handling the provisioning and configuration of the network element.

Claim 21 (Currently Amended): A ~~machine-readable~~ storage medium that provides instructions for handling exceptions within a multi-processor system, which when executed by a machine, causes the machine to perform operations comprising:

receiving an exception within a processor which is one of a plurality of processors of the multi-processor system which is implemented within a control card of a network element for routing data in networks, wherein each of the plurality of processors in the multi-processor system shares a memory within the multi-processor system, wherein the memory includes a

common interrupt handling vector address space shared by the plurality of the processors and a dedicated interrupt handling vector address space for each of the plurality of the processors, and

executing one or more instructions at an address associated with a type of the received exception within the common interrupt handling vector address space of the memory, wherein the one or more instructions cause the processor to modify based on an identification of the processor an execution flow of the received exception to execute an interrupt handler located within a respective dedicated interrupt handling vector address spaces associated with the processor,

wherein the plurality of processors includes a first processor and a second processor, the first processor executing a first operating system and the second processor executing a second operating systems the second operating system being different from the first operating systems, and

wherein the first processor along with the first operating system is configured to handle routing of data received within the network element and the second processor along with the second operating system is configured to handle provisioning and configuration of the network element;

wherein the first operating system is a real-time operating system handling the routing of data within the network element and the second operating system is a non real-time operating system handling the provisioning and configuration of the network element.

Claim 23 (Currently Amended): A ~~machine-readable~~ storage medium of claim 21~~2~~, wherein each of the operating systems is associated with a dedicated interrupt handling vector address spaces associated with a processor executing the respective operating system.

Claim 24 (Currently Amended): A ~~machine-readable~~ storage medium of claim 21, further comprising determining the identification of the processor by reading a bit of a register within the processor without having to access the memory.

Claim 25 (Currently Amended): A ~~machine-readable~~ storage medium of claim 24, wherein the register is part of a cache throttling register of the processor, and wherein a dedicated bit of the register is used to indicate the identification of the processor while at least a portion of remaining bits of the register is used for cache throttling purposes.

Claim 26 (Currently Amended): A ~~machine-readable~~ storage medium of claim 21, wherein determining the identification of the processor comprises:

communicating during an initialization of the processor with a memory controller coupling the processors and the memory to retrieve the identification of the processor from the memory controller; and

storing the retrieved identification of the processor in the register within the processor.

Claim 27 (Currently Amended): A ~~machine-readable~~ storage medium of claim 21, wherein each entry of the common interrupt handling vector space is associated with a different type of

exceptions of the multi-processor system, and wherein a result of executing the instructions in the common interrupt handling vector space and the identification of the processor receiving the exception determine the dedicated interrupt handling vector space associated with the processor.

Allowable Subject Matter

7. Claims 1, 3-12, 14-16, 21 and 23-27 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Haresh Patel whose telephone number is (571) 272-3973. The examiner can normally be reached on Monday, Tuesday, Thursday and Friday from 10:00 am to 8:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Haresh Patel

March 16, 2006

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